METHOD AND SYSTEM FOR LOW POWER REFRESH OF DYNAMIC RANDOM ACCESS MEMORIES

ABSTRACT OF THE DISCLOSURE

A method and system for operating a DRAM device in either a high power, full density mode or a low power, half density mode. In the full density mode, each data bit is stored in a single memory cell, and, in the half density mode, each data bit is stored in two memory cells that are refreshed at the same time to permit a relatively slow refresh rate. When transitioning from the full density mode to the half density mode, data are copied from each row of memory cells storing data to an adjacent row of memory cells. The adjacent row of memory cells are made free to store data from an adjacent row by remapping the most significant bit of the row address to the least significant bit of the row address, and then remapping all of the remaining bits of the row address to the next highest order bit.